B.E (FT) END SEMESTER ARREAR EXAMINATIONS – Apr / May 2025		
Computer Science and Engineering		
Fourth Semester		
CS6107 – COMPUTER ARCHITECTURE		
(Regulation 2018 - RUSA)		
Time: 3 Hours	Answer ALL Questions	Max. Marks 100
Note: Assume data, if required		
PART-A (10 x 2 = 20 Marks)		
1.	Specify the instruction format for I type instruction, give example.	2
2.	How does pseudo addressing mode work?	2
3.	Identify the process in ALU for a conditional branch instruction.	2
4.	Discuss the following instruction of MIPS: slt, addi	2
5.	Design a 4 bit adder using carry look ahead generation logic.	2
6.	Apply bit pair recoding on the multiplier 1001000010.	2
7.	Identify the conditions to be satisfied for forwarding.	2
8.	Compare and contrast static vs dynamic branch prediction.	2
9.	Why are interface circuits used by I/O devices? Give their role.	2
10.	Is daisy chaining advantageous? Give reasons.	2
PART – B (8 x 8 = 64 marks) **(Answer any 8 questions)**		
11.	Write a MIPS assembly language program to find the sum of squares of elements stored in an array.	8
12.	Explain how functions are handled in MIPS architecture. Illustrate with a function to find Fibonacci series of the given number.	8
13.	Summarize the different addressing modes used in MIPS architecture and explain the address computation with example.	8
14.	Design a simple functional unit that can perform and, or and add and explain.	8
15.	Design a sequential multiplier. Simulate to find 5*-4.	8

16.	Illustrate the division algorithm with a sequential circuit and flowchart. Simulate it for 8/3	8
17.	Explain the working of floating point addition with a circuit and flowchart.	8
18.	Draw the data path for sw $s3, 4($s1) and explain.	8
19.	Design datapath for R type with the control signals generated by main control unit and also tabulate the description for the possible states of the control signals	8
20.	Elaborate the different cache mapping techniques. Illustrate the mapping techniques with suitable examples.	8
21.	Identify the various bus standards used. Explain their features and advantages.	8
22.	How interrupts help in I/O transfer where processor is relieved, explain with neat illustration.	8
	PART – C (2 x 8 = 16 marks)	
23.	Present the dynamic scheduling hardware, explain the algorithm with necessary illustrations.	8

24.	Identify the dependencies and hazards in the following code sequence. Use pipeline diagram to indicate how forwarding provides solutions for the hazards identified. Insert NOP if required.
	LD R3, 0(R2)
	ADD R4, R4, R3
	LD R4, 32(R5)
	SUB R1, R3, R4
	SUB R3, R4, R2
	LD R4, 32(R3)
	SD R4, 50(R1)
		8